

### **REMARKS**

The applicants have carefully considered the official action mailed on November 24, 2008, and the reference applied therein. In the official action, claims 1-10, 12-19, 21-27, and 29-33 were rejected under 35 U.S.C. §102(b) as allegedly anticipated by Kim et al. (The Structure of a Compiler for Explicit *and* Implicit Parallelism).

Claims 1-10, 12-19, 21-27, and 29-33 remain pending in this application, of which claims 11, 20, and 28 were canceled in a prior response, and claims 1, 19, 24, 31, and 33 are independent. Favorable reconsideration is respectfully requested in view of the following remarks.

The applicants respectfully submit that independent claim 1 is allowable over the art of record. Independent claim 1 is directed to a method of compiling a program that, *inter alia*, determines a misspeculation cost value for at least one speculative parallel thread candidate, and selects a set of speculative parallel threads from a set of speculative parallel thread candidates based on the misspeculation cost value. Kim et al. do not describe or suggest determining a misspeculation cost value for at least one speculative parallel thread candidate, and selecting a set of speculative parallel threads from the set of speculative parallel thread candidates based on a misspeculation cost value, as recited in claim 1.

Instead, Kim et al. describe speculative processor extensions of an explicit type and an implicit type. As discussed in the prior response, implicit parallelism refers to “extract(ing) parallelism speculatively from a sequential instruction stream” and explicit parallelism refers to “execut(ing) explicit parallel code sections as a multiprocessor.” See *Kim et al.*, Abstract. Kim et al. are capable of generating both explicit and implicit

threads, but Kim et al. more specifically address issues related to integrating a parallelizing processor with a code generator and determining when it is more appropriate to generate explicit threads versus implicit threads. *Id.* When selecting threads, Kim et al. describe overhead considerations related to thread management costs (*see Kim et al., section 2.2, pages 4-5*), two of which include speculative storage overflow and subroutine conversion (*see Kim et al., section 4, page 10*). While the aforementioned overheads are fairly described as thread management costs, the applicants respectfully submit that none of these overhead considerations are fairly construed as misspeculation costs, much less a method to determine a misspeculation cost value for speculative parallel thread candidates, and selecting a set of speculative parallel threads from the set of candidates based on the misspeculation cost value, as recited in claim 1.

The examiner appears to contend (*See page 6 of the official action*) that Kim et al. describe determining a misspeculation cost value for at least one speculative parallel thread candidate. In particular, the examiner appears to contend that speculative storage overflow (*see Kim et al., section 4, pages 9-10*) is a concept synonymous with and/or related to a misspeculation cost value. However, Kim et al. clearly describe that the speculative storage overflow relates to a management consideration of implicit thread overhead rather than any concept(s) associated with negative consequences of thread selection, much less misspeculation and/or determining a misspeculation cost value. Speculative storage overflow occurs when the speculative state of Kim et al. build up an excess capacity of storage, which is more fairly construed as a management/maintenance consideration rather than a concept related to misspeculation.

In fact, Kim et al. describe additional maintenance-related costs, such as subroutine conversion overheads in the preprocessing step when adding instructions for explicit threads. The one or more types of overhead considerations described by Kim et al. allow a decision regarding whether parallel code sections should be executed as either implicit or explicit threads. For example, unlike a misspeculation cost value, Kim et al. describe that, in the event of detection of speculative storage overflow (a maintenance consideration) the compiler chooses explicit thread execution to avoid a processor stall condition.

While the applicants appreciate that the pending claims must be “given their broadest reasonable interpretation,” such interpretation is also to be “consistent with the specification.” *Phillips v. AWH Corp.*, 415 F.3d 1303, 75 USPQ2d 1321 (Fed. Cir. 2005) (emphasis added). Additionally, the United States Patent and Trademark Office (USPTO) employs the “broadest reasonable interpretation” standard, which includes “giving claims their broadest reasonable construction “in light of the specification as it would be interpreted by one of ordinary skill in the art.” *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1364 [, 70 USPQ2d 1827] (Fed. Cir. 2004) (emphasis added). The applicants respectfully submit that the examiner’s contention that speculative storage overflow is allegedly equivalent to and/or related to a misspeculation cost and/or a misspeculation cost value is neither consistent with the specification nor proper in view of an interpretation by one of ordinary skill in the art. In fact, Kim et al. neither recite the term misspeculation nor describe any circumstances that determine a quantity as a function of the likelihood of a data dependency violation within a thread candidate or an amount of computation required to recover from such a dependency violation.

Instead, Kim et al. focus on maintenance costs and various overhead considerations associated with thread selection choices, which are not the same as calculating a quantity that is a function of the likelihood of a data dependency violation, much less a misspeculation cost value. An interpretation by persons having ordinary skill in the art would not find concepts related to speculative storage overflow described by Kim et al. as being consistent with the instant specification. As recited in claim 1, the term “misspeculation” includes the modifier “mis,” which should not be ignored if the claims are to be properly examined. Additionally, unlike the base-term “speculation,” the specific modifier “mis” and the term “misspeculation” are clearly defined by the applicants in, at least, paragraph [0033] of the specification, which is unrelated to speculatively written values, storage overflow, and/or maintenance costs associated with the overheads described by Kim et al.

If the examiner’s assertion regarding the alleged equivalence of a misspeculation cost value, as recited in claim 1, and the speculative storage overflow described by Kim et al., then the claims will neither “conform to the invention as set forth in the remainder of the specification,” nor will “the claims...find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description,” as required pursuant to 37 C.F.R. 1.75(d)(1). While “[c]laims are not to be read in a vacuum, and limitations therein are to be interpreted in light of the specification in giving them their ‘broadest reasonable interpretation’,” at least one result from maintaining the examiner’s assertion is that the claims will not enjoy the benefit of a reasonable interpretation, particularly in view of the specification and the

meaning understood by persons having ordinary skill in the art. *In re Marosi*, 710 F.2d at 802, 218 USPQ at 292 (Fed. Cir. 1983) (emphasis added).

Thus, because Kim et al. fail to describe or suggest determining a misspeculation cost value for at least one speculative parallel thread candidate, independent claim 1 necessarily fails to anticipate Kim et al. Accordingly, the rejection of claims 2-10, and 11-18 dependent upon independent claim 1, must also be withdrawn for the foregoing reasons.

Independent claims 19, 24, and 31 are also allowable over the art of record for reasons similar to those set forth above in connection with independent claim 1. In particular, each of claims 19, 24, and 31 is directed to an article of manufacture storing machine readable instructions, an apparatus, or a system that, *inter alia*, determines a misspeculation cost value for at least one of a speculative parallel thread candidate, and selects a set of speculative parallel threads from a set of speculative parallel thread candidates based on the misspeculation cost value. None of the cited references describes or suggests determining a misspeculation cost value for at least one of a speculative parallel thread candidate, and selecting a set of speculative parallel threads from a set of speculative parallel thread candidates based on the misspeculation cost value, as recited in claim 19, 24, and 31, and claims dependent therefrom.

The applicants also submit that independent claim 33 is allowable over the art of record. Independent claim 33 recites, *inter alia*, determining a likelihood that a data dependency violation will occur, determining an amount of computation required to recover from the data dependency violation, and selecting at least one of a set of speculative parallel thread candidates based on a lowest likelihood of misspeculation.

Kim et al. neither describes nor suggests determining a likelihood that a data dependency violation will occur, determining an amount of computation required to recover from the data dependency violation, and selecting at least one of a set of speculative parallel thread candidates based on a lowest likelihood of misspeculation, as recited in claim 33.

Similar to the reasons set forth above in connection with independent claim 1, Kim et al. are completely devoid of a misspeculation, much less selecting at least one of the set of thread candidates based on a lowest likelihood of misspeculation. The examiner refers to section 4 of Kim et al. as allegedly teaching selecting at least one of the set of thread candidates based on a lowest likelihood of misspeculation, but instead Kim et al. describe techniques of implicit and explicit thread selection in view of maintenance costs and/or overhead rather than consequences due to misspeculation.

Thus, for at least the foregoing reasons, the applicants respectfully submit that all pending claims are now in condition for allowance. If there are any remaining issues in this application, the applicants urge the examiner to contact the undersigned attorney at the number listed below.

The Commissioner is hereby authorized to charge any fees which may be required under 37 CFR 1.16 or 1.17 to Deposit Account No. 50-2455.

Respectfully submitted,

/Peter J. Cesarz/  
Peter J. Cesarz  
Reg. No. 61,190  
Attorney for Applicants  
150 S. Wacker Drive, Suite 2100  
Chicago, IL 60606  
(312) 580-1020

**January 19, 2009**